MEMS1082

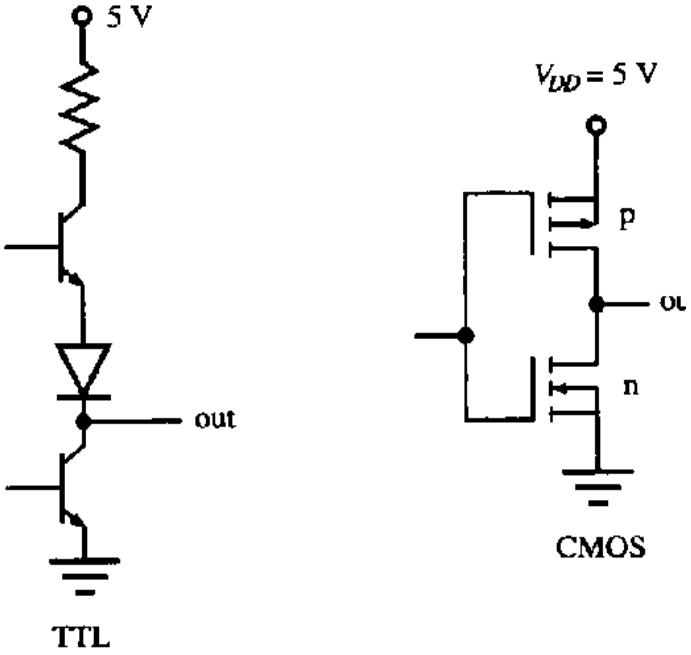
Chapter 6 Digital Circuit 6-6

TTL and CMOS ICs

- TTL and CMOS output circuit

totem pole configuration

When the upper transistor is forward biased and the bottom transistor is off, the output is high. The resistor, transistor, and diode drop the actual output voltage to a value typically about 3.4 V. When the lower transistor is forward biased and the top transistor is off, the output is low.
The TTL device sources current when there is a high output and sinks current when the output is low.



TTL and CMOS output circuits.

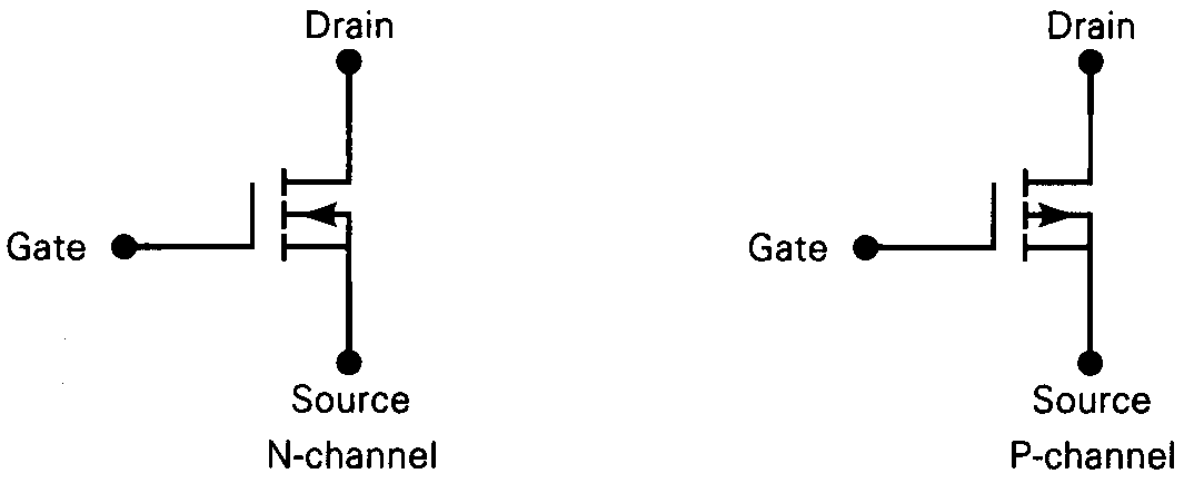
When input is high, the p-type transistor (top) is off, n-type is on. So the output is pulled low. The device sinks current

When input is low, the n-type transistor (bottom) is off, p-type is on. So the output is pulled high. The device sources current.

TTL device dissipates power continuously regardless of whether the output is high or low.

The MOSFET and MOSFET switching states

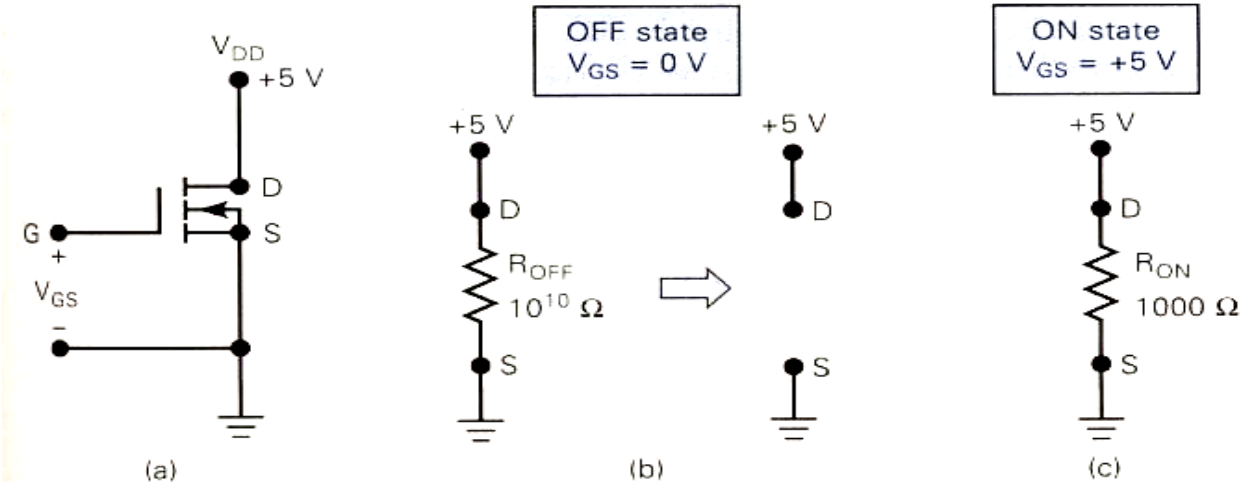
Schematic symbols for enhancement MOSFETs.



There are presently two general types of MOSFETs: depletion and enhancement.
MOS digital ICs use enhancement MOSFETs exclusively
The direction of the arrow indicates either P- or N-channel. The symbols show a broken line between the source and drain to indicate that there is normally no conducting channel between these electrodes.
Symbol also shows a separation between the gate and the other terminals to indicate the very high resistance (typically around $10^{12}\ \Omega$) between the gate and channel.

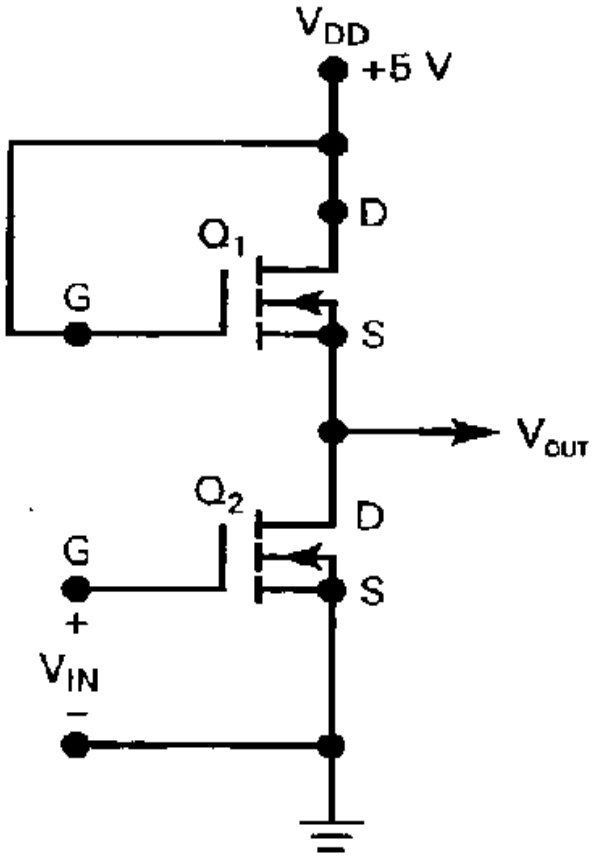
The MOSFET and MOSFET switching states

N-channel MOSFET switching states.



	Drain-to-Source Bias	Gate-to-Source Voltage (V_{GS}) Needed for Conduction	R_{ON} (Ω)	R_{OFF} (Ω)
P-channel	Negative	Typically more negative than −1.5 V	1000 (typical)	10^{10}
N-channel	Positive	Typically more positive than +1.5 V	1000 (typical)	10^{10}

N-MOS Inverter



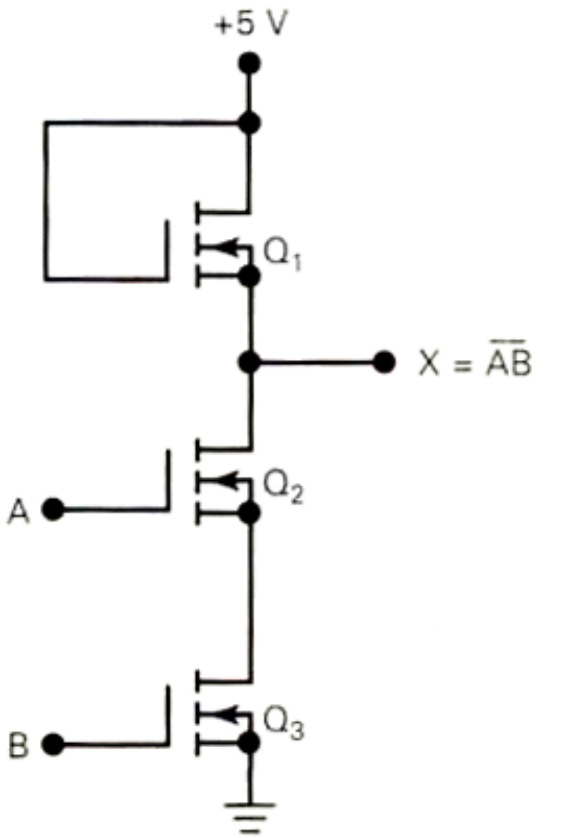
(a)

V_{IN}	Q_1	Q_2	$V_{OUT} = \overline{V_{IN}}$
0 V (logic 0)	R_{ON} = 100 kΩ	R_{OFF} = 10^{10} Ω	+5 V (logic 1)
+5 V (logic 1)	R_{ON} = 100 kΩ	R_{ON} = 1 kΩ	+0.05 V (logic 0)

(b)

N-MOS NAND Gate

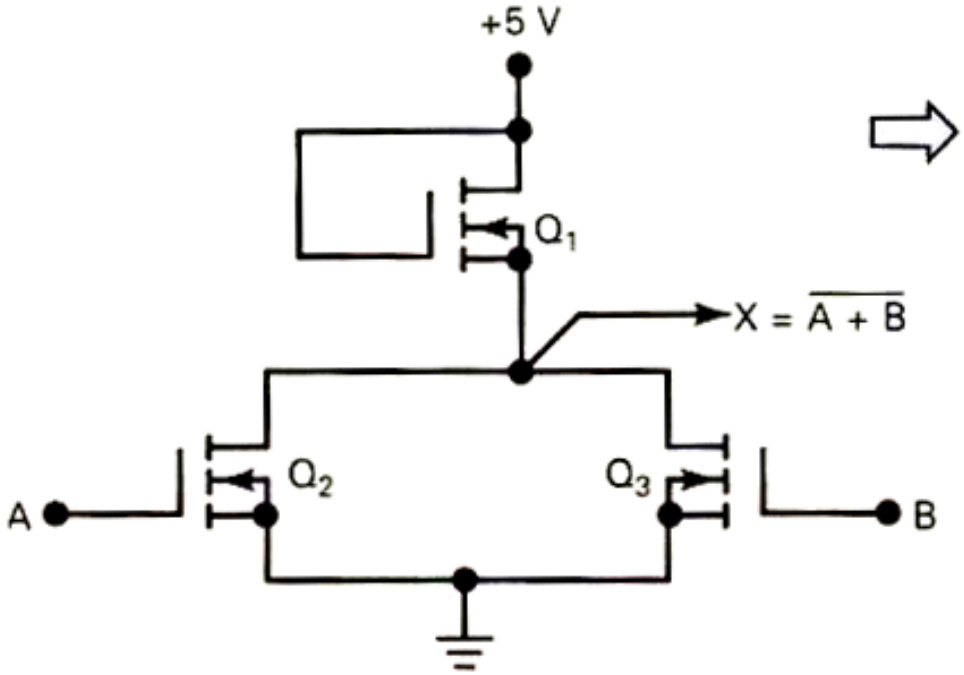
(a) N-MOS NAND gate;

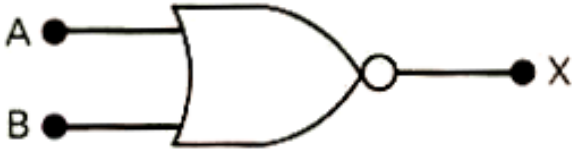


(a)

A	B	X
LOW (0 V)	LOW	HIGH
HIGH (+5 V)	LOW	HIGH
LOW	HIGH	HIGH
HIGH	HIGH	LOW

N-MOS NOR Gate



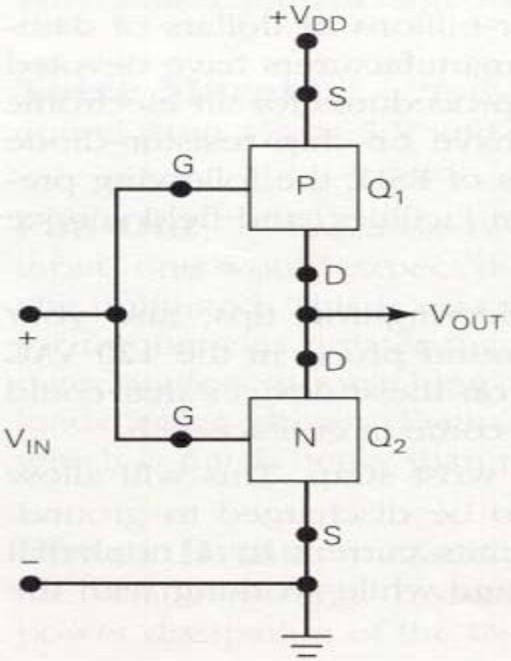


A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

CMOS Logic

The complementary MOS (CMOS) logic family uses both P- and N- channel MOSFETs in the same circuit to realize several advantages over the P-MOS and N-MOS families. The CMOS is faster and consumes even less power than the other MOS families.

Basic CMOS INVERTER.

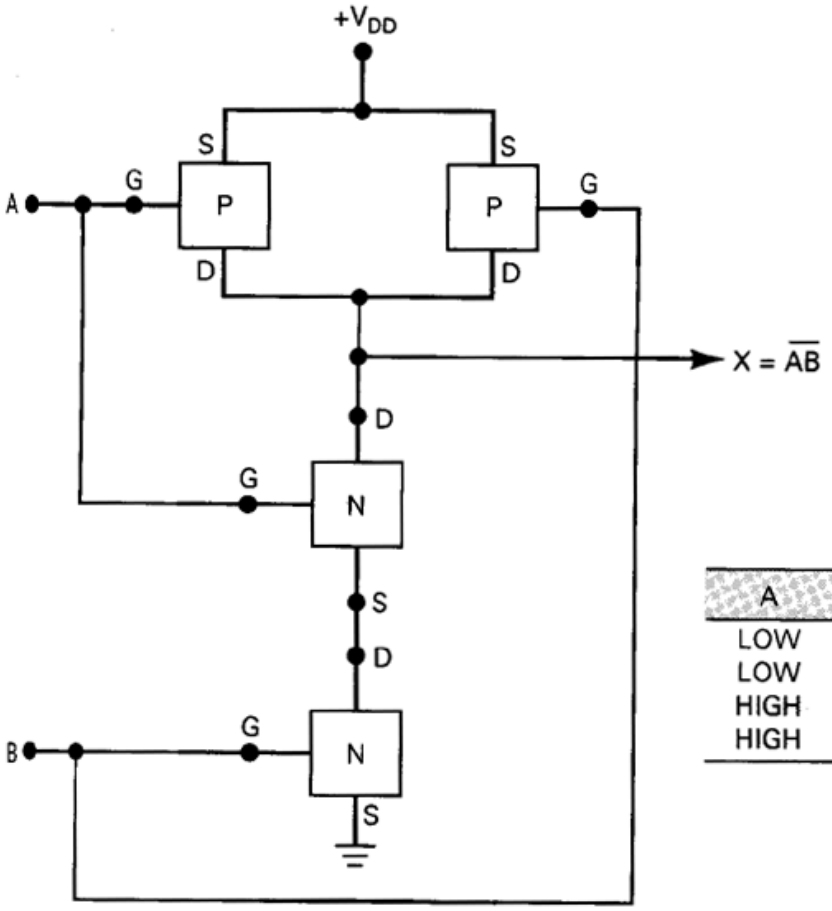


V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	$\simeq 0$ V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	$\simeq +V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

CMOS Logic

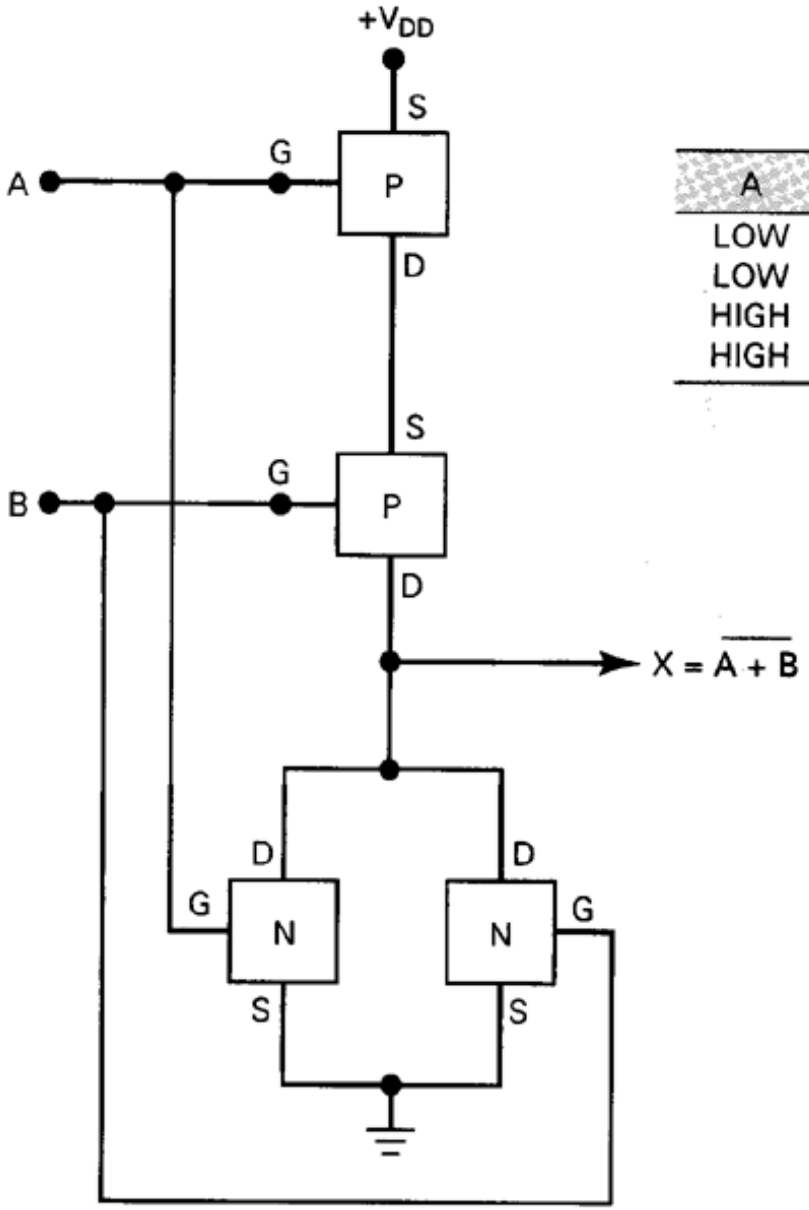
CMOS NAND gate.



A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

CMOS Logic

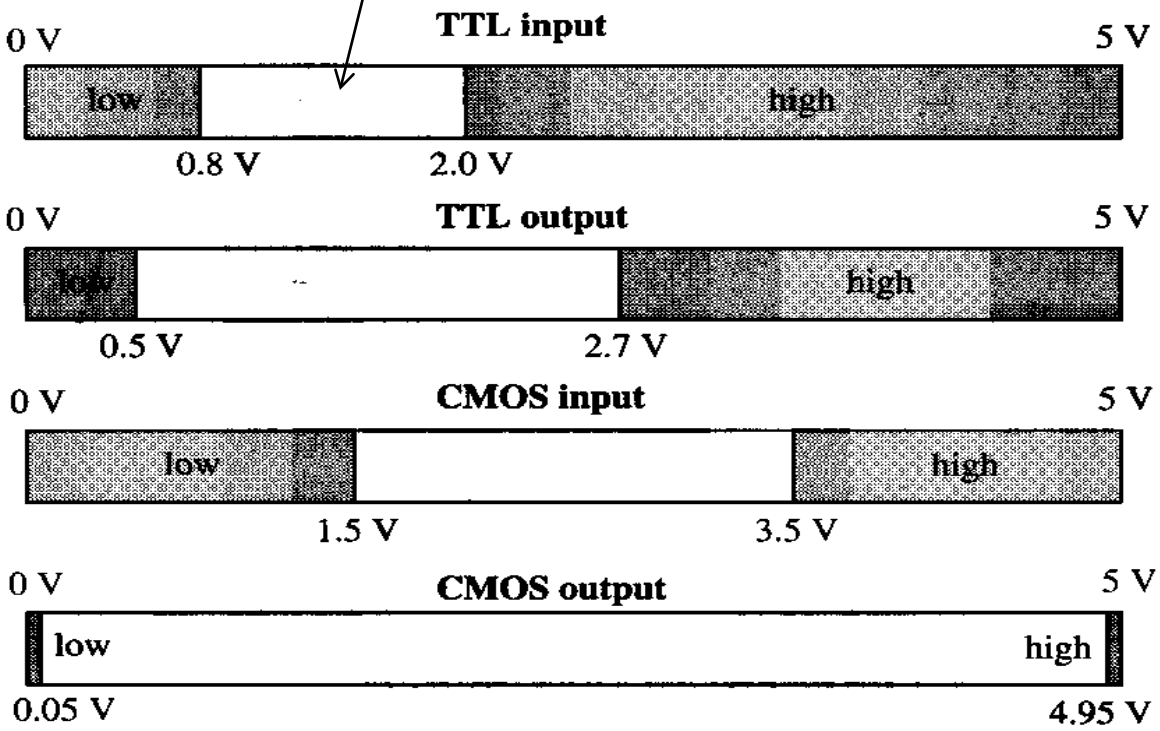
CMOS NOR gate.



A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

TTL and CMOS ICs

Logic low (L) or (0) **Undefined** **Logic high (H) or (1)**



TTL and CMOS input and output levels.

TTL and CMOS ICs

- When interfacing digital devices, in addition to understanding the voltage levels, it is also important to know the input and output current characteristics of the devices. Important characteristics are the amount of current a device can source (produce) when the output is high and the amount of current the device can sink (draw) when the output voltage is low.
  - I_{OL} – "low-level output current" for sinking capability when the output voltage is low
  - I_{OH} – "high-level output current" for sourcing capability when the output voltage is high

Advantages of CMOS devices

- When an output is unloaded or connected to other CMOS devices, CMOS requires power only when an output switches its logic state. Therefore, CMOS is useful in battery-operated applications where power is limited
- The wide power supply range of CMOS (3-18 V) provides more design flexibility and allows use of less tightly regulated power supplies.

- Disadvantages of CMOS:
  - CMOS is sensitive to static discharge ; the devices are easily damaged
  - CMOS requires negligible input current, but its output current is also small compared to TTL. This limits the ability of CMOS to drive large TTL fan-out or other high current devices.

Manufacturer IC data sheet

- Labeling in TTL: AAxxyzz,
  - AA is the manufacturer's prefix (SN for TI and others; DM for National Semiconductor);
  - xx distinuishes between military (xx = 54) and industrial (xx = 74) quality;
  - y distinguishes between different internal designs
    - no letter: standard TTL;
    - L: low-power dissipation;
    - H: high-power dissipation;
    - S: Schottky type; Schottky devices have faster switching speeds and require less power.
    - AS: advanced Schottky,
    - LS: low-power Schottky;
    - ALS: advanced low-power Schottky); and
  - zz is the device number in the data book.

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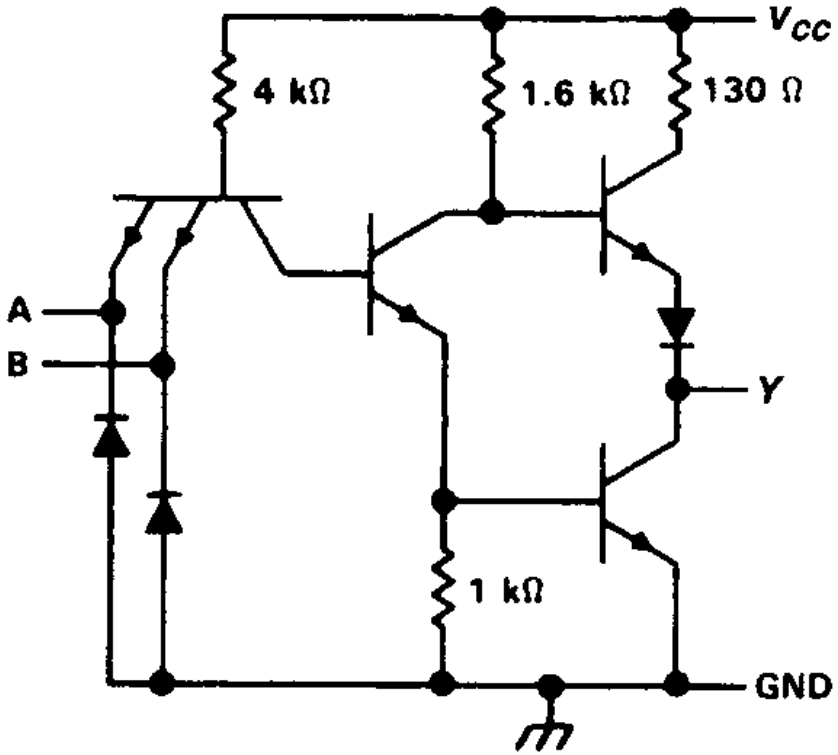
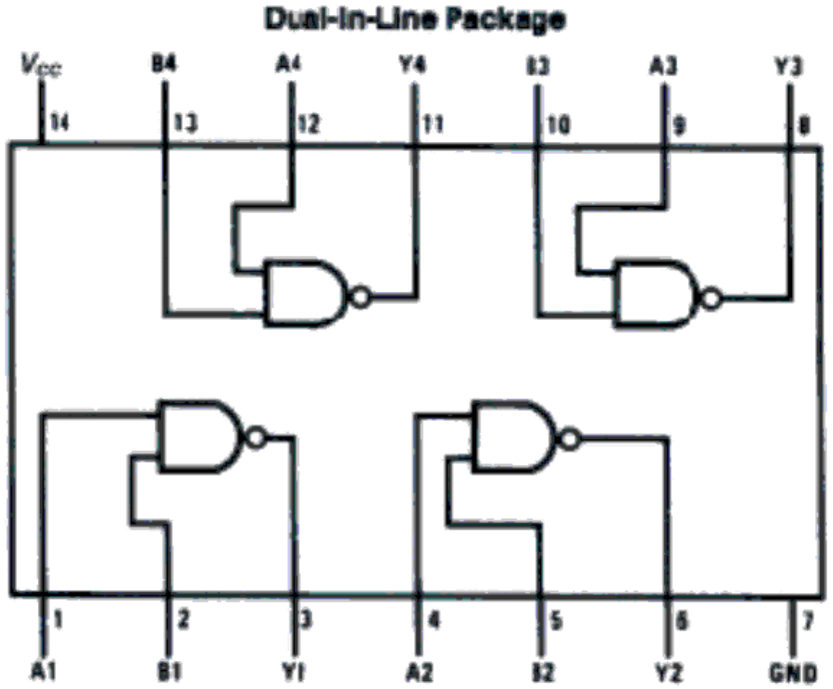
  - zz is the device number in the data book.

Manufacturer IC data sheet

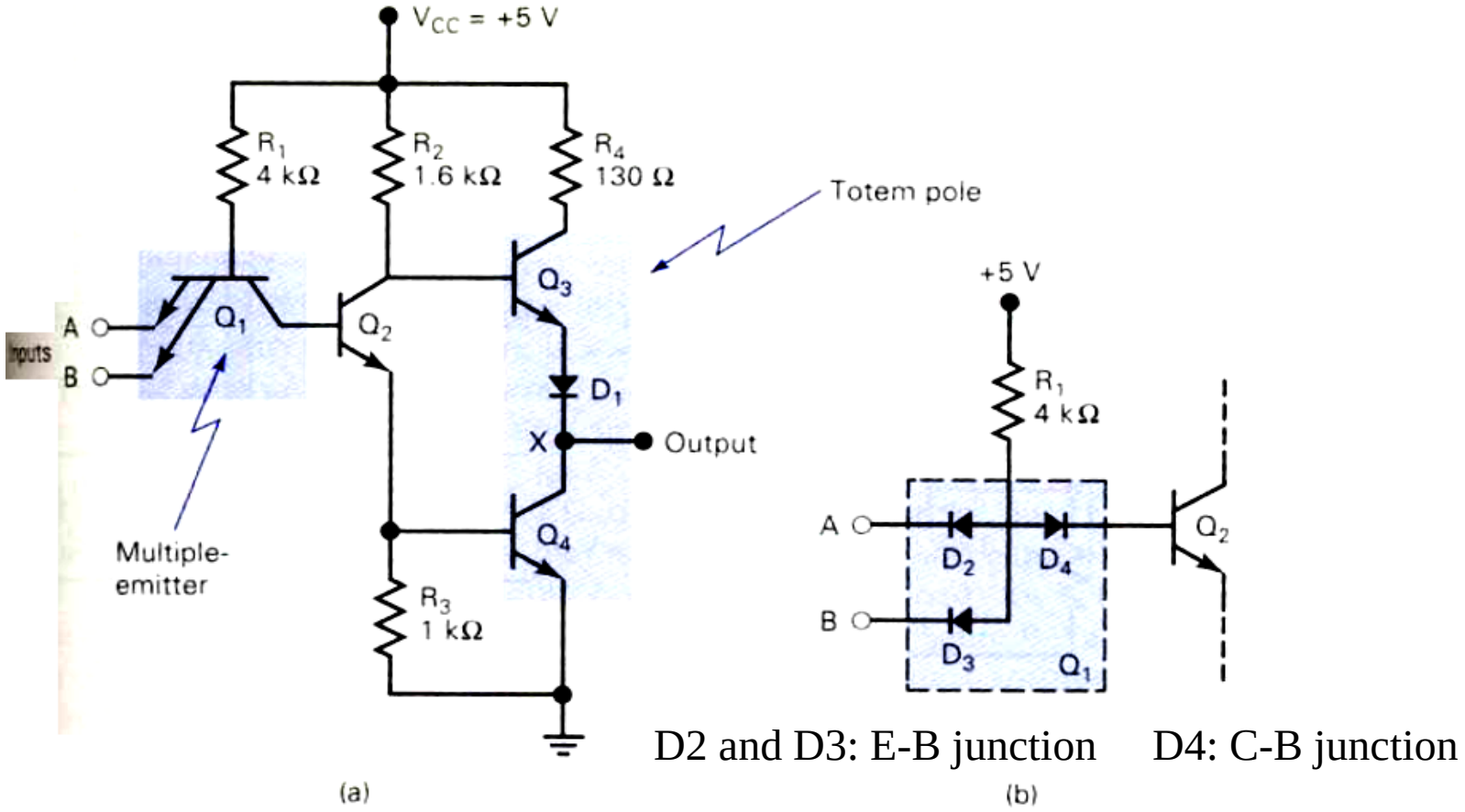
- CMOS devices are available in the 40XXB series and the 74CXX series.
- 74CXX series is pin compatible with the TTL 74XX series. There are also different varieties of the 74CXX family that provide different speed and power characteristics.
  - 74HCXX (high-speed CMOS),
  - 74ACXX (advanced CMOS), and
  - 74HCTXX and 74ACTXX (high-speed CMOS with TTL threshold).

NAND gate internal design and QUAD NAND gate IC pin-out





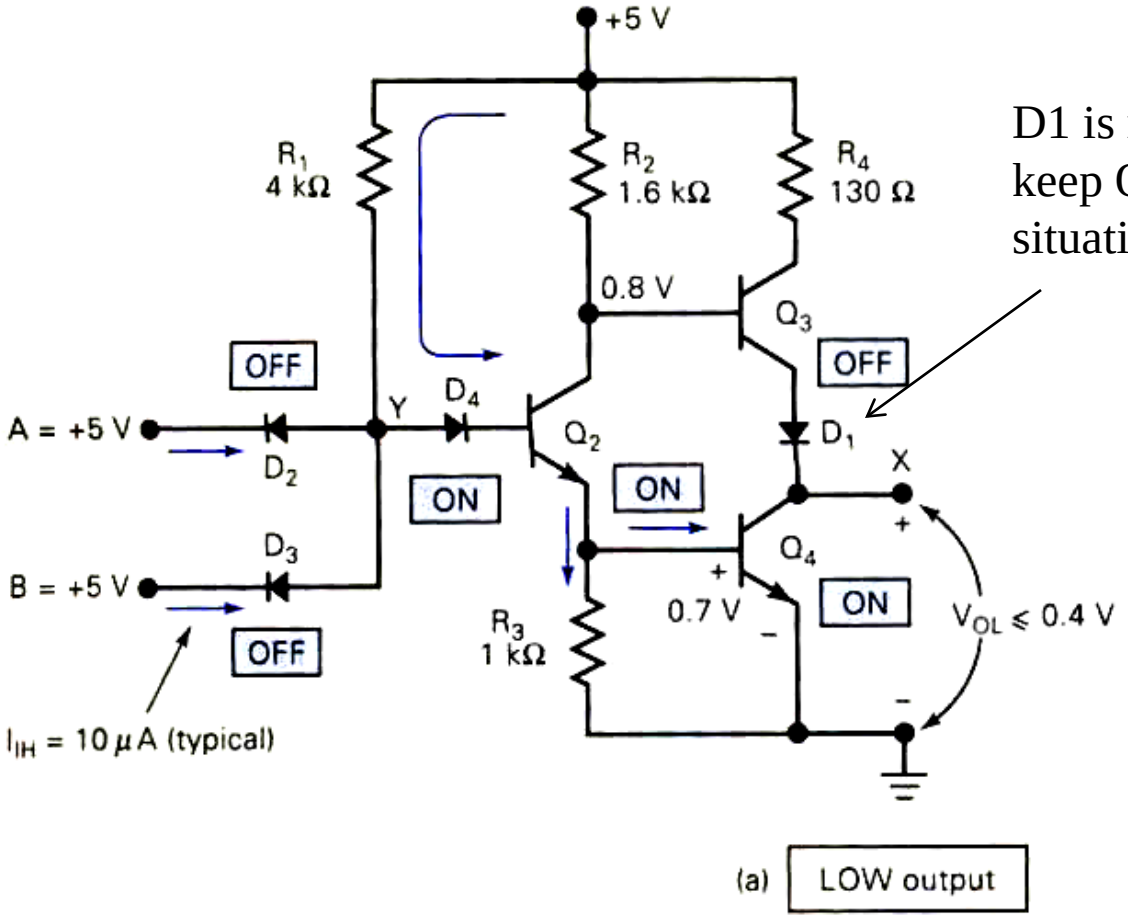
NAND gate internal design and its operation



D2 and D3: E-B junction D4: C-B junction

(a) Basic TTL NAND gate; (b) diode equivalent for Q_1.

NAND gate internal design and its operation

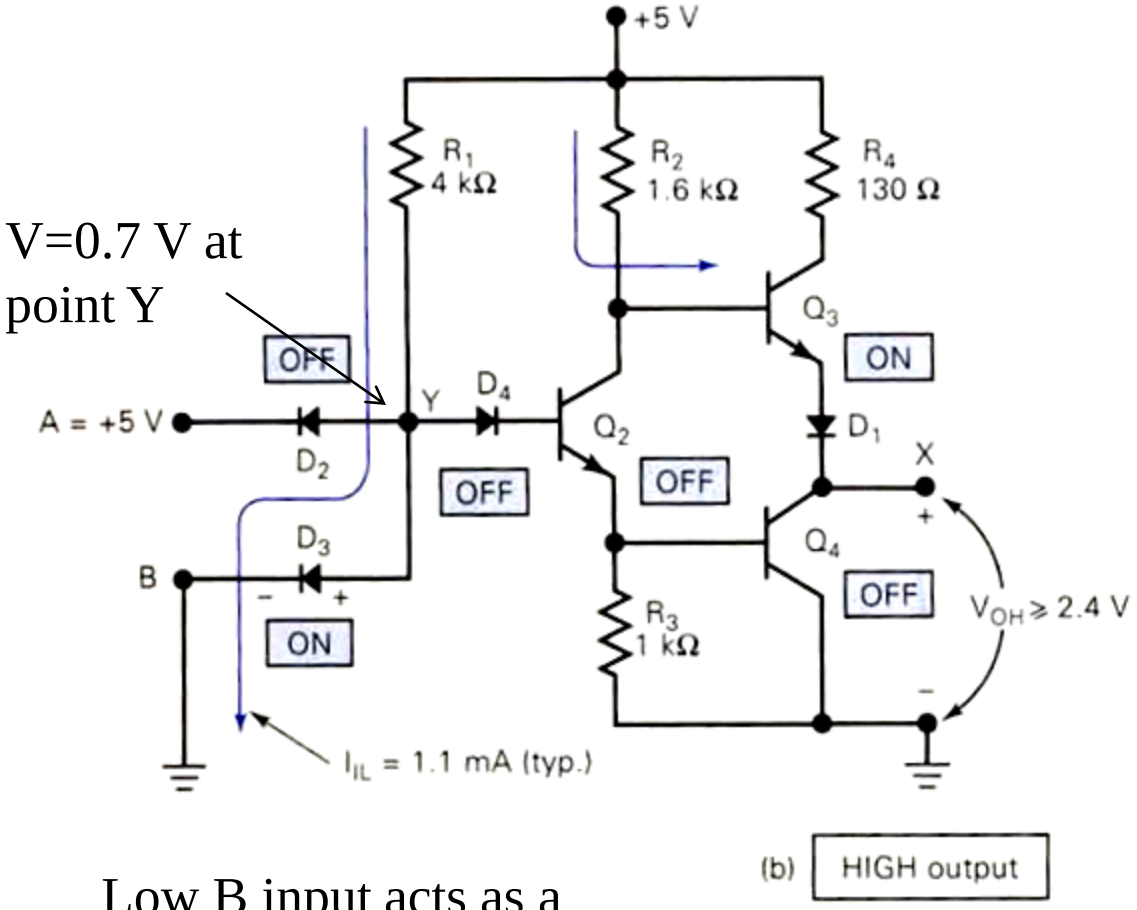


(a) LOW output

D1 is needed to keep Q3 off in this situation

Input conditions	Output conditions
A and B are both HIGH (≥2 V)	Q_3 OFF
Input currents are very low I_{IH} = 10 μA	Q_4 ON so that V_X is LOW (≤0.4 V)

NAND gate internal design and its operation



(b) HIGH output

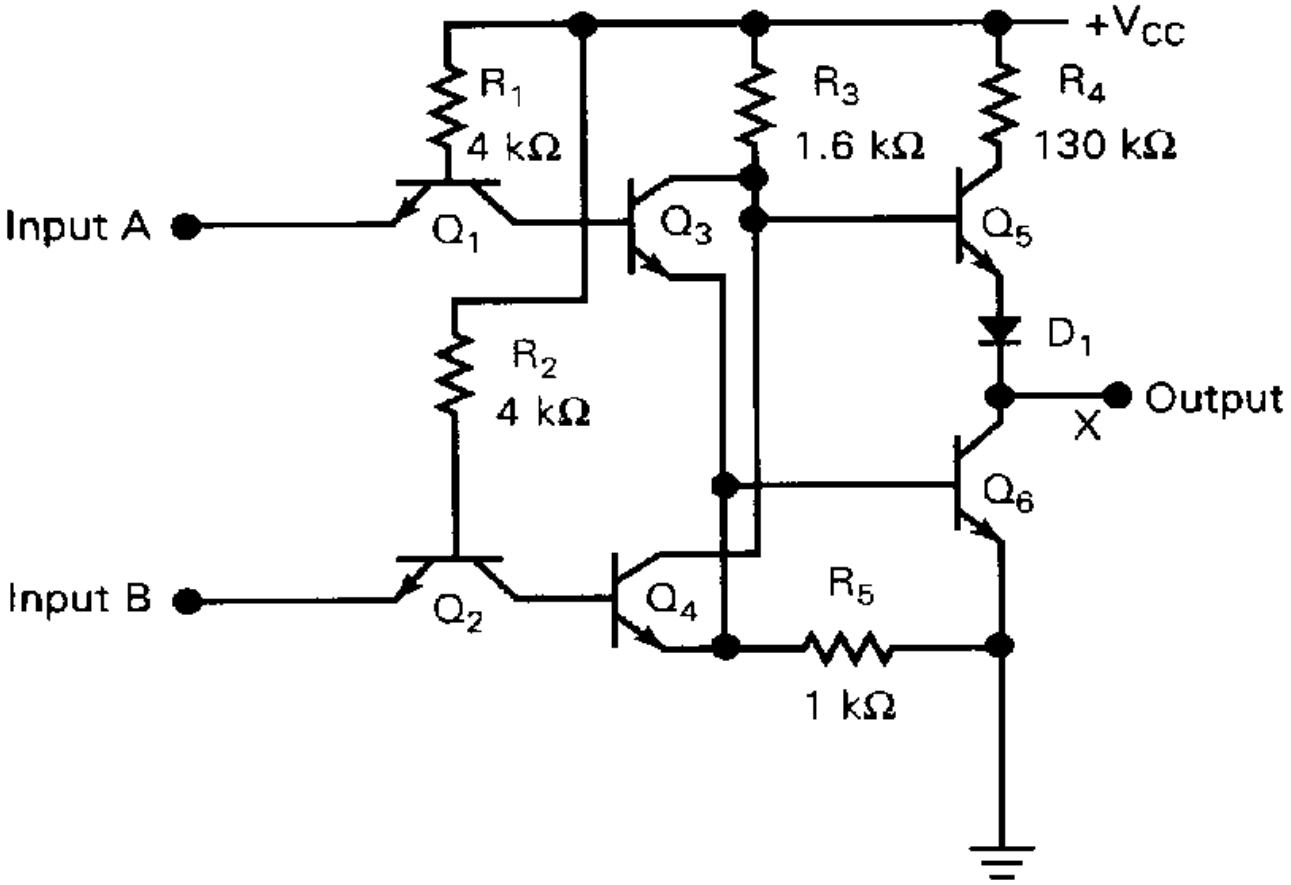
V=0.7 V at point Y

Input conditions	Output conditions
A or B or both are LOW (≤ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal. I_{IL} = 1.1 mA	Q_3 acts as emitter-follower and $V_{OH} \geq 2.4$ V, typically 3.6 V

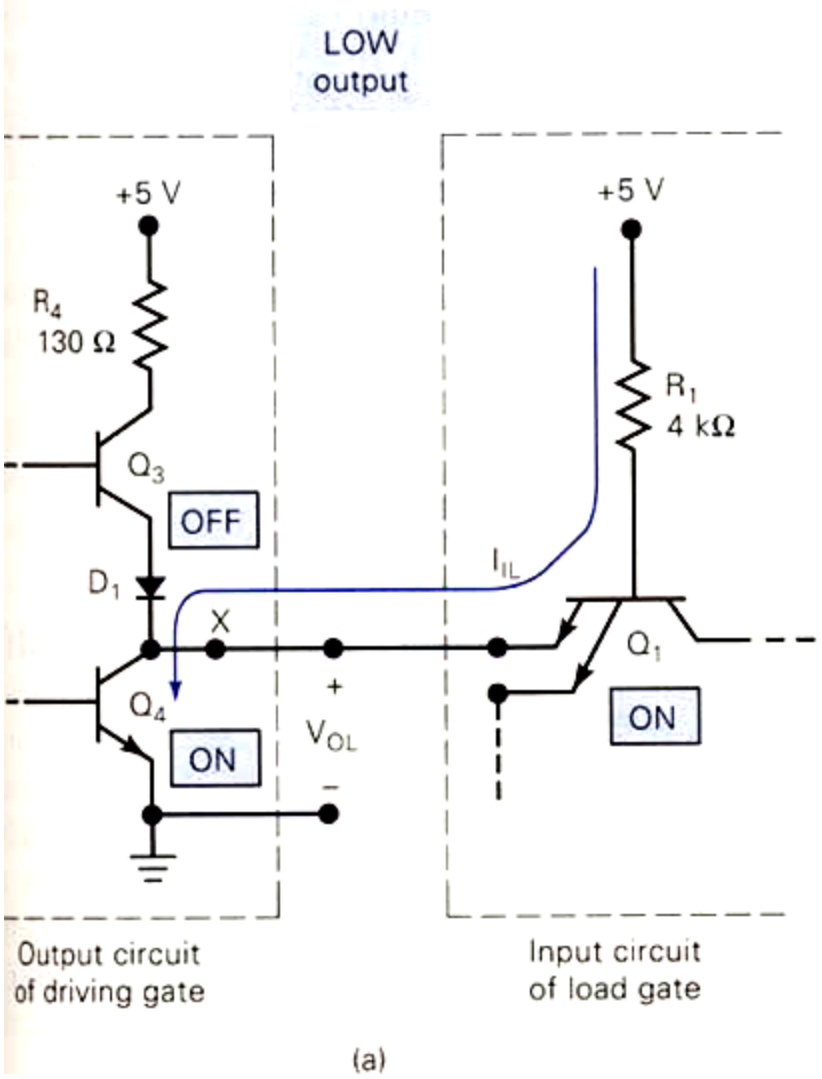
Low B input acts as a sink to ground to this current

TTL NOR gate internal design

TTL NOR gate circuit.

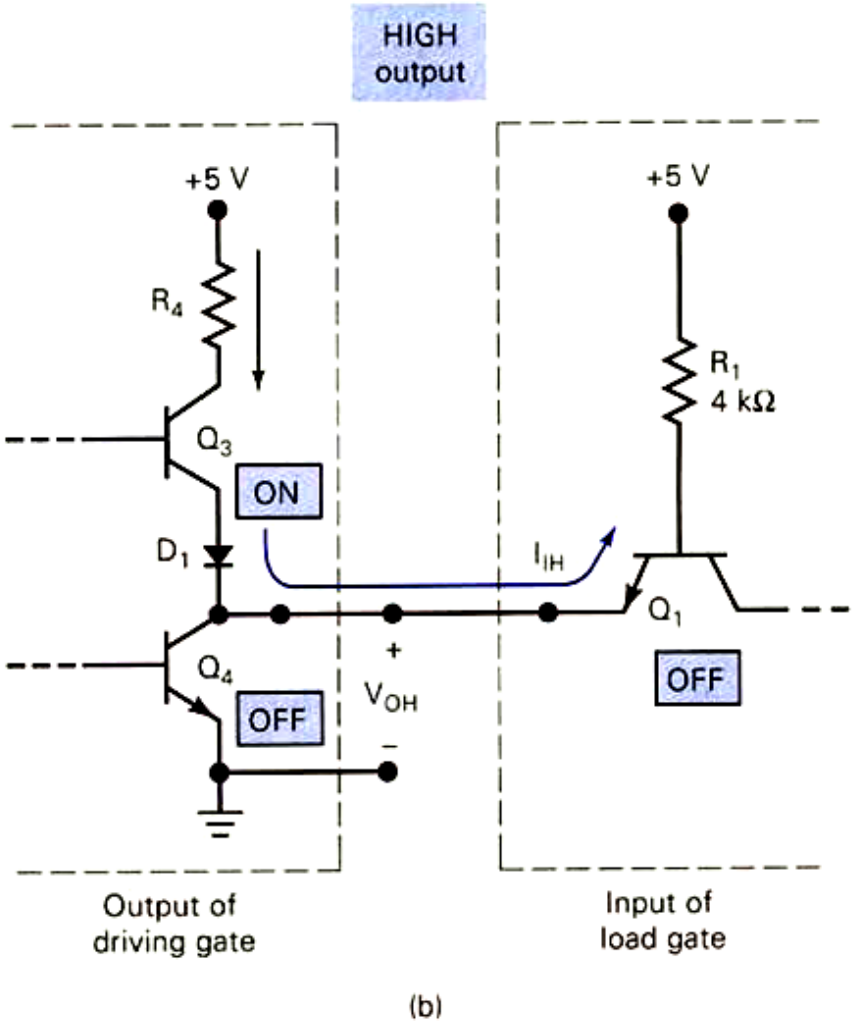


Current sinking action



Q4 is the current-sinking transistor or the pull-down transistor

Current sourcing action

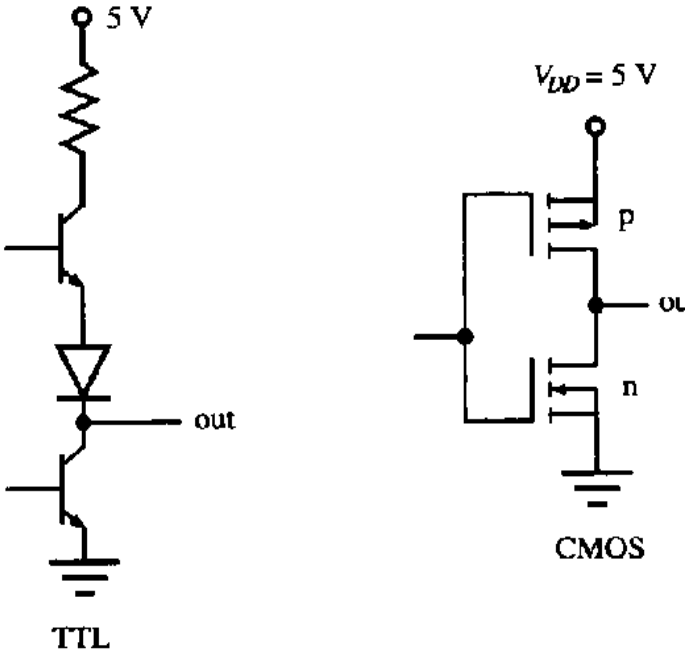


(b)

Q3 is the current-sourcing transistor
Or the pull-up transistor

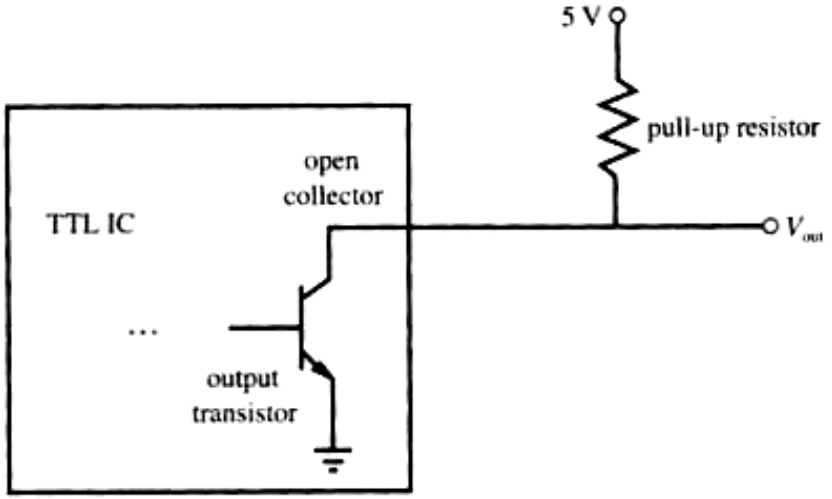
Digital IC output configurations

totem pole configuration



TTL and CMOS output circuits.

Open-collector output

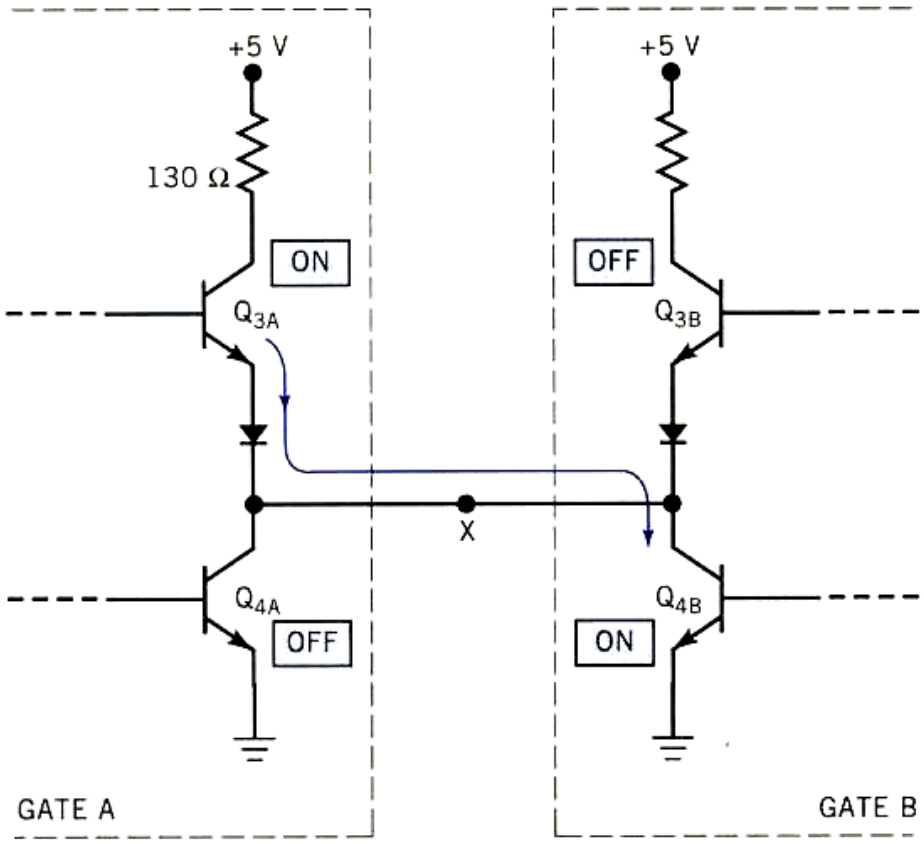


Open-collector output with pull-up resistor.

When the output transistor is saturated, V_{out} is low
When it is in cutoff, V_{out} is high

Digital IC output configurations

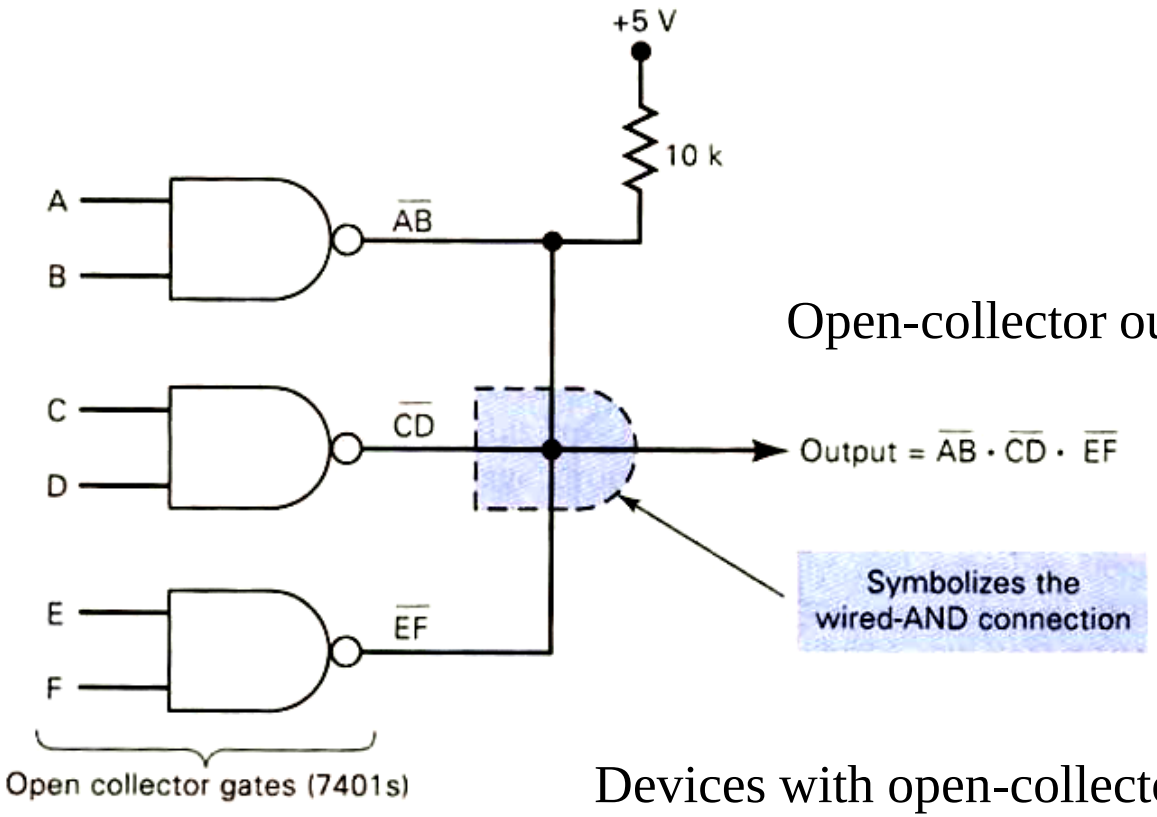
Caution! Totem pole outputs should not be tied together



Totem-pole outputs tied together can produce harmful current through Q_4.

Digital IC output configurations

Wired-AND operation using open-collector gates.



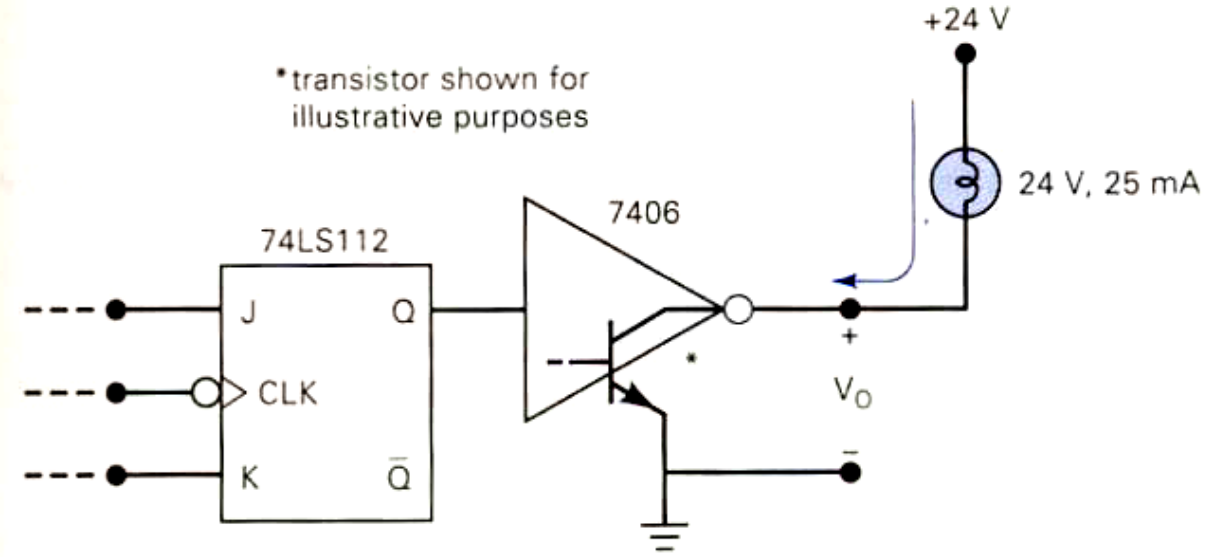
Open-collector output

Devices with open-collector (OC) outputs can have their outputs connected together safely

Digital IC output configurations

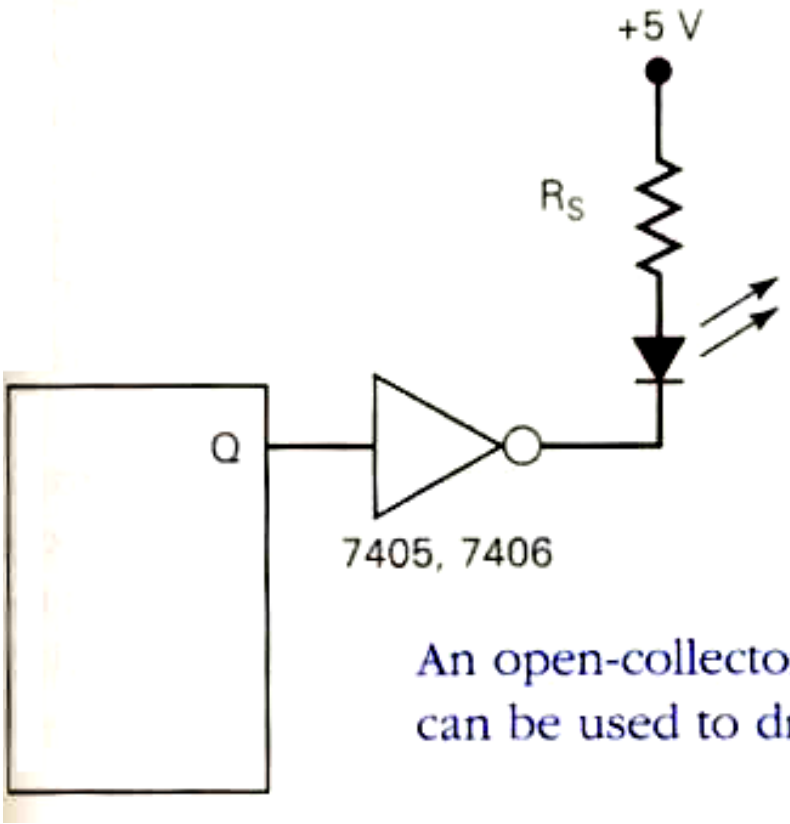
Open collector buffer/drivers:

A buffer, or a driver or a buffer/driver is designed to have a greater output current and/or voltage capability than ordinary logic circuit. Buffer/driver ICs are available with totem pole outputs and with open-collector outputs



An open-collector buffer-driver drives a high-current, high-voltage load.

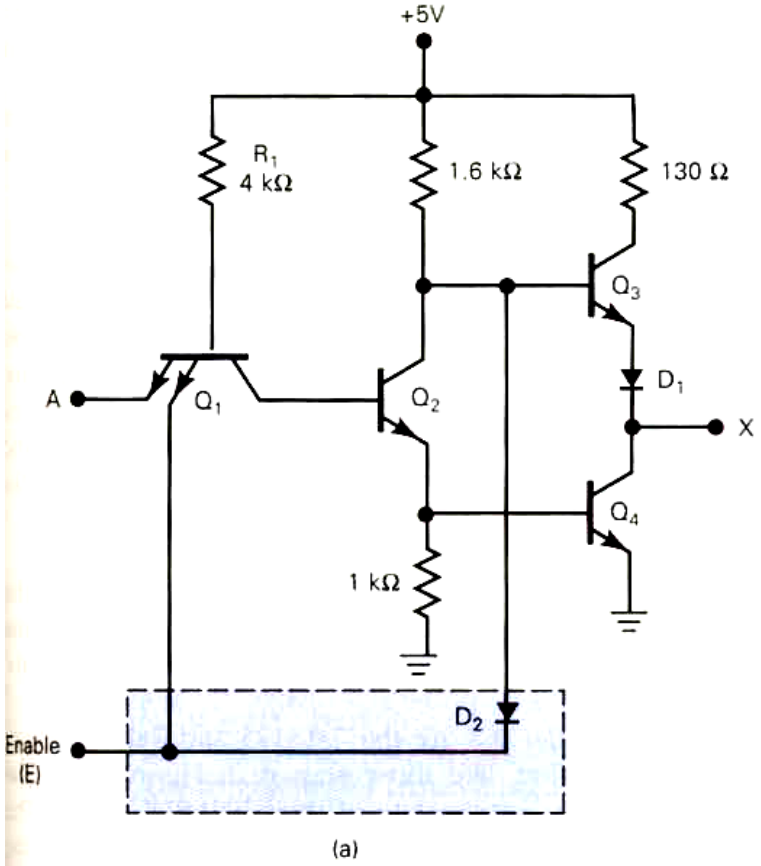
Digital IC output configurations



An open-collector output
can be used to drive an LED indicator.

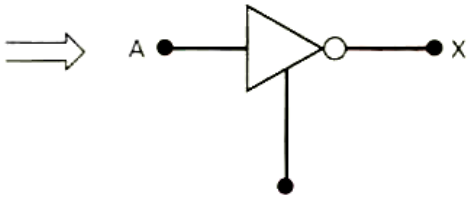
Digital IC output configurations

Tristate TTL inverter



(a)

Tristate TTL allows three possible output states: HIGH, LOW and high impedance (Hi-Z)



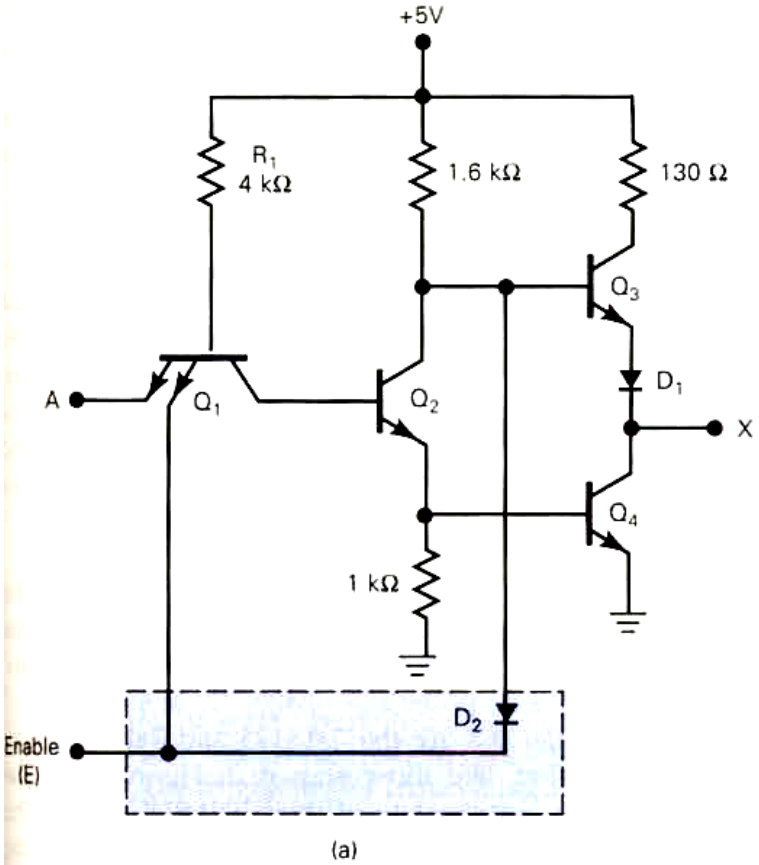
Operating conditions

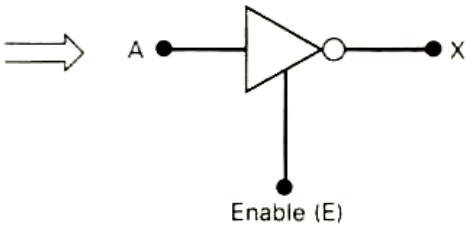
ENABLE (E)	OUTPUT
HIGH	Enabled: operates as an INVERTER
LOW	Disabled: output is Hi-Z state. Input A has no effect.

(b)

Operating conditions

Digital IC output configurations





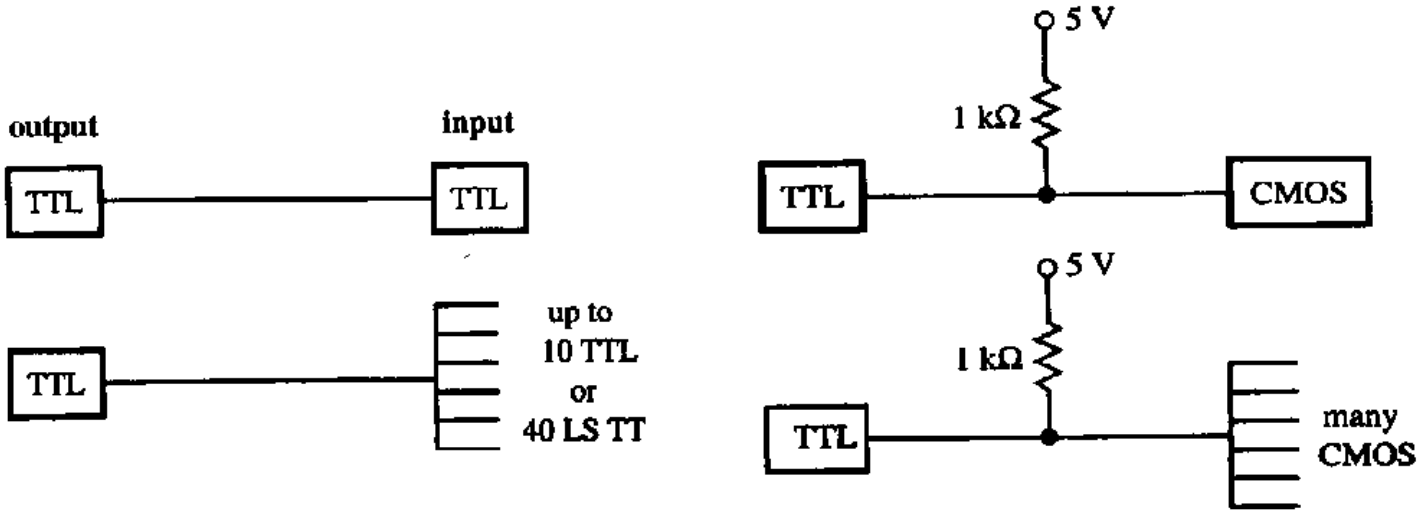
The Enabled State With E = 1 the circuit operates as a normal inverter because the HIGH voltage at E has no effect on Ql or D2. In this enabled condition, the output is simply the inverse of logic input A.

The Disabled State (Hi-Z): When E = O the circuit goes into its Hi-Z state regardless of the state of logic input A. The LOW at E forward-biases the emitter-base junction of Ql and shunts the Rl Current away from Q2 so that Q2 turns off, which turns Q4 off. The LOW at E also forward-biases diode D2 to shun current away from the base of Q3, so that Q3 also turns off.

(b)

Operating conditions

Interfacing TTL and CMOS devices

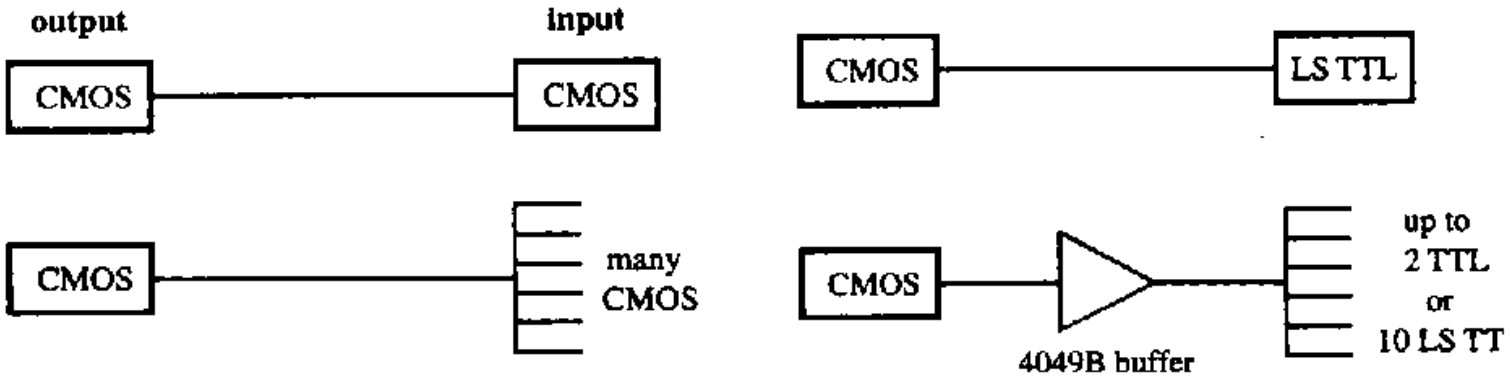


Interfacing TTL to digital devices.

The output of a TTL device sinks current when it is low and sources current when it is high. The TTL low sink current (IoJ is the limiting factor when interfacing to multiple TTL inputs. A TTL output can drive up to 10 standard TTL inputs or up to 40 Low-power Schottky (LS) TTL inputs.

TTL outputs are easy to interface to CMOS due to the insulating gate input, which draws no steady state current. It is necessary only to ensure voltages match when connecting TTL outputs to CMOS inputs.

Interfacing TTL and CMOS devices

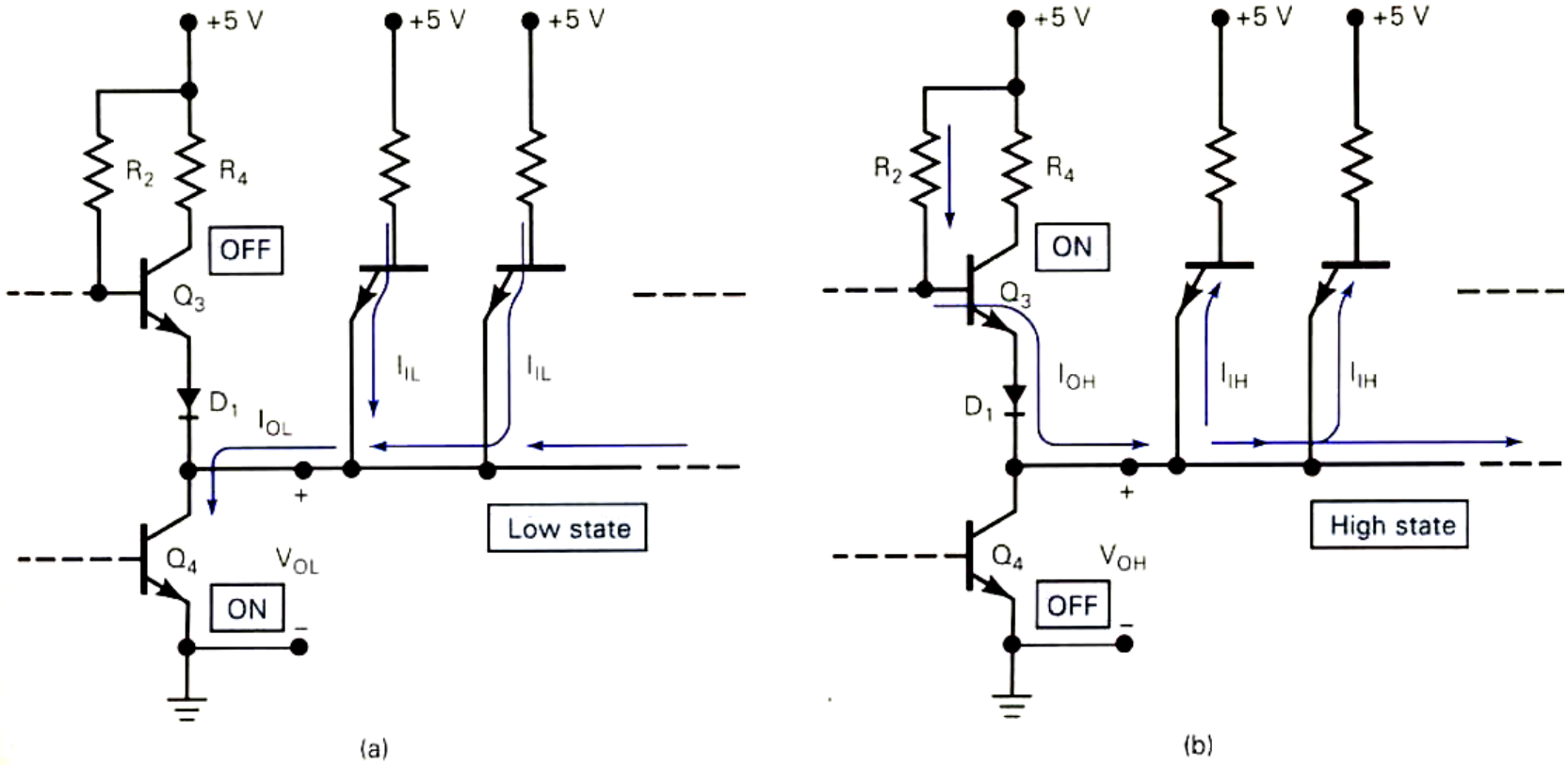


Interfacing CMOS to digital devices.

When using ICs of one logic family exclusively, you need not be concerned with voltage levels and current drives as long as the fan-out is less than 10 for TTL (CMOS can be higher).

CMOS is better for general use because it draws no current unless switching, and the output swings nearly from ground to the positive supply value. However, at high frequency, CMOS can dissipate nearly the power required by an equivalent TTL circuit.

TTL Loading and fan-out



Currents when a TTL output is driving several inputs.